FuturePlus Systems Corporation

Agilent Technologies
Innovating the HP Way

Premier Solution Partner

32/64 bit PCI Pinout

For use with Agilent Technologies Logic Analyzers and FuturePlus Systems Software

REV 3.0

About the Pinout 3
What you will need to analyze PCI 3
64 bit PCI 3
32 bit PCI 3
Where to place the MICTOR connectors on the target 4
The Termination Network 4
PCI Signal Assignment 5
Routing and Re-pinning Information 5
GNT#, REQ# and IDSEL signals 5
LOGIC ANALYZER POD 1 6
LOGIC ANALYZER POD 2 6
LOGIC ANALYZER POD 3 7
LOGIC ANALYZER POD 4 7
LOGIC ANALYZER POD 5 8
LOGIC ANALYZER POD 6 8
E5346A 9
E5346A/E5351A Mechanical Dimensions 10
AMP Mictor-38 Connector 10
Shroud Mechanical Information 12
Technical Support 12

About the Pinout

This document describes the pinout for the AMP Mictor 38 pin header to a 32 or 64 bit PCI local bus. Following this pinout will allow the user to use the E5346A High-Density Termination Adapter Cable and the FuturePlus Systems 64 bit PCI software for PCI analysis with an Agilent logic analyzer. *This pinout does not support the 16510/511 or 16540 series of logic analyzers. It **does** support the 1655x, 167xx, 1670, and 1660 series of logic analyzers.*

What you will need to analyze PCI

64 bit PCI

- 3 AMP 2-767004-2 surface mount connectors mounted on the target board and routed to the PCI Local bus.
- 3 E5346A High-Density Adapter Cables from FuturePlus Systems or Agilent, 6 logic analyzer PODS required.
- A software license FS1101 from FuturePlus Systems for **16500** Agilent logic analyzers and **portable** logic analyzers or a software license FS1106 from FuturePlus Systems for **16700** Agilent logic analyzers.

32 bit PCI

- 2 AMP 2-767004-2 surface mount connectors mounted on the target board and routed to the PCI Local bus.
- 2 E5346A High-Density Adapter Cables from FuturePlus Systems or Agilent, 4 logic analyzer PODS required.
- A software license FS1101 from FuturePlus Systems for **16500** Agilent logic analyzers and **portable** logic analyzers or a software license FS1106 from FuturePlus Systems for **16700** Agilent logic analyzers.

The Mictor-38 connectors will be referred to as #1 and #2 and #3 (#3 for 64 bit only). Each Mictor-38 connector connects to two logic analyzer PODS, an EVEN numbered POD and an ODD numbered POD. Pins 1,2 and 4 on both Mictor-38 connectors are no connects. Pin 3 and pins 39-43 should be connected to GROUND.

The FuturePlus Systems software FS1101 consists of configuration files and an Inverse Assembler. ***For details on the configuration files and the Inverse Assembler please refer to the FS2001 data sheet and manual (***www.futureplus.com**/**technical support***)***

The FuturePlus Systems software FS1106 consists of configuration files and uses B4605B Tool Development Kit to decode PCI bus signals into easy to understand mnemonics. The transaction decode software performs the following functions:

- Decode all PCI command and cycle types
- Provide insight into the data transfer by indicating burst length, byte enables and number of byte enables. These are all color coded to match the command.
- Color the transaction per the command for easy correlation. The colors used by the software are as follows:
    - Memory transactions: Green
    - I/O transactions: Yellow
    - Configuration transactions: Blue

- Interrupt Acknowledge, Special Cycle transactions and the DAC cycle: Purple
- Idle and Wait cycles: White

♦ Determine the following performance metrics:

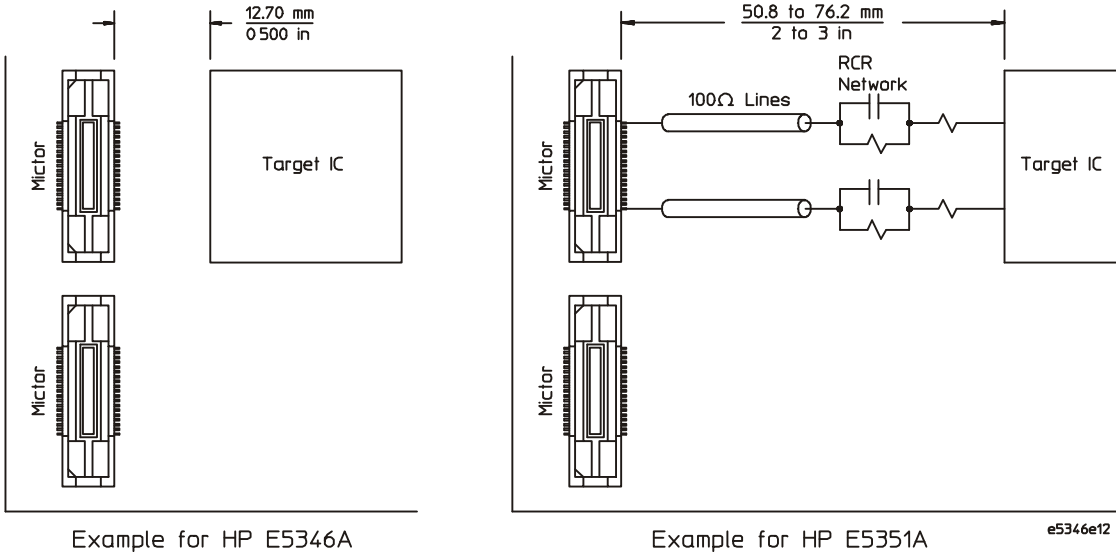
- Latency: data to data and address to first data. This label is color coded to indicate spec compliance.
- Byte Enable Efficiency
- Total Efficiency
- Overall Time Efficiency

♦ Provide a quick summary of the traffic through the Command/Address and Length/Termination labels.

♦ Remove the input data set to present an uncluttered display

Where to place the MICTOR connectors on the target

The recommended placement of the mictor connectors is at either end of the bus segment. The mictors should be placed at the end of as short a stub as possible daisy chained off either end of the bus. If there is not enough room to place the mictors **0.5 inches** from the target then an alternate method may be used. That is, to place the logic analyzer termination circuitry on the target and then extend the etch from the end of the termination circuitry over to the mictor connectors. The connection from the mictors to the logic analyzer must then be done with the **E5351A.** The E5346A contains the logic analyzer termination circuitry, the E5351A does not.



The Termination Network

The termination network consists of a 249 ohm resistor in series with the parallel combination of a 90K ohm resistor and a 8.2pF capacitor. The components are placed as shown in the drawing above. If the etch from the network to the mictor connector is less than one inch, the impedance of the etch can be in the 60-75 ohm range. If it is longer, it should be controlled at 100 ohms.

If the termination network is placed on the target then the stub should be 0.5" or less. In general, the stub must be << 50% of the wavelength of the rise time of the signal for it to be treated as a lumped C rather than a transmission line.

PCI Signal Assignment

FuturePlus Systems will supply a configuration file with the FS1101/FS1106 product that matches the following pinout. However it should be noted that the pinout could be re-pinned by the user for **16700 systems** in order to match etch lengths and control skew. The configuration for (FS1101)**16500 systems must not be** changed.

Routing and Re-pinning Information

In order to control skew all etch lengths should be near equal. If it makes sense from a layout point of view, the signals may be re-pinned on the mictor connectors. The user would then only need to modify the included configuration file to match the actual layout. The following restrictions apply.

- The clock cannot be re-pinned to a signal pin
- Bit re-ordering can be used to put the command/AD signals back in order . If the AD signals are RE-ORDERED then the user will not be able to use the IN RANGE feature in the triggering menu for address range triggering.
- The CYCLE variable will need to be bit re-ordered to match the supplied symbols in the configuration file. (This is not a difficult task).

GNT#, REQ# and IDSEL signals

It is recommended that the target system GNT# lines and optionally the REQ# and IDSEL signals of the target PCI local bus be connected to the unused or user pins. This may make debugging and performance analysis easier.

LOGIC ANALYZER POD 1

Mictor-38 #1 Pin Number ODD POD	Logic Analyzer channel number	PCI Signal name
6	CLK/16	IRDY#
8	15	AD15
10	14	AD14
12	13	AD13
14	12	AD12
16	11	AD11
18	10	AD10
20	9	AD09
22	8	AD08
24	7	AD07
26	6	AD06
28	5	AD05
30	4	AD04
32	3	AD03
34	2	AD02
36	1	AD01
38	0	AD00

LOGIC ANALYZER POD 2

Mictor-38 #1 Pin Number EVEN POD	Logic Analyzer channel number	PCI Signal name
5	CLK/16	FRAME#
7	15	AD31
9	14	AD30
11	13	AD29
13	12	AD28
15	11	AD27
17	10	AD26
19	9	AD25
21	8	AD24
23	7	AD23
25	6	AD22
27	5	AD21
29	4	AD20
31	3	AD19
33	2	AD18
35	1	AD17
37	0	AD16

LOGIC ANALYZER POD 3

Mictor-38 #2 Pin Number ODD POD	Logic Analyzer channel number	PCI Signal name
6	CLK/16	PCI Clock
8	15	unused*
10	14	INTD#
12	13	INTC#
14	12	INTB#
16	11	INTA#
18	10	RST#
20	9	C/BE3#
22	8	C/BE2#
24	7	C/BE1#
26	6	C/BE0#
28	5	DEVSEL#
30	4	STOP#
32	3	LOCK#
34	2	PERR#
36	1	SERR#
38	0	PAR

*This pin is unused and can be connected to any signal and assigned by the user in the Format menu**.**

LOGIC ANALYZER POD 4

Mictor-38 #2 Pin Number EVEN POD	Logic Analyzer channel number	PCI Signal name
5	CLK/16	TRDY#
7	15	USER7
9	14	USER6
11	13	USER5
13	12	USER4
15	11	USER3
17	10	USER2
19	9	USER1
21	8	SDONE
23	7	SBO#
25	6	C/BE7#
27	5	C/BE6#
29	4	C/BE5#
31	3	C/BE4#
33	2	PAR64
35	1	ACK64#
37	0	REQ64#

LOGIC ANALYZER POD 5

Mictor-38 #3 Pin Number ODD POD	Logic Analyzer channel number	PCI Signal name
6	CLK/16	unused*
8	15	AD47
10	14	AD46
12	13	AD45
14	12	AD44
16	11	AD43
18	10	AD42
20	9	AD41
22	8	AD40
24	7	AD39
26	6	AD38
28	5	AD37
30	4	AD36
32	3	AD35
34	2	AD34
36	1	AD33
38	0	AD32

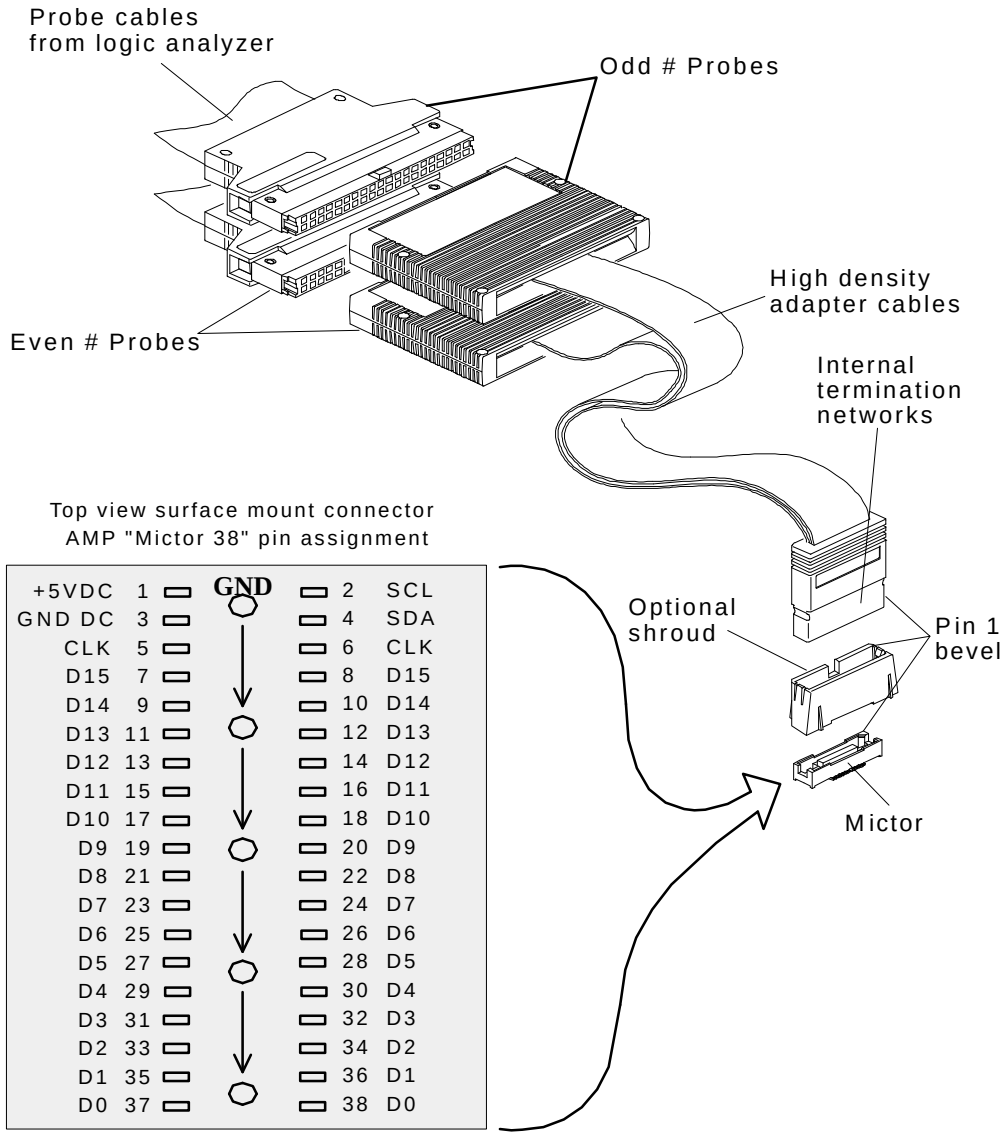
***This pin is unused and can be connected to any signal and assigned by the user in the Format menu.**

LOGIC ANALYZER POD 6

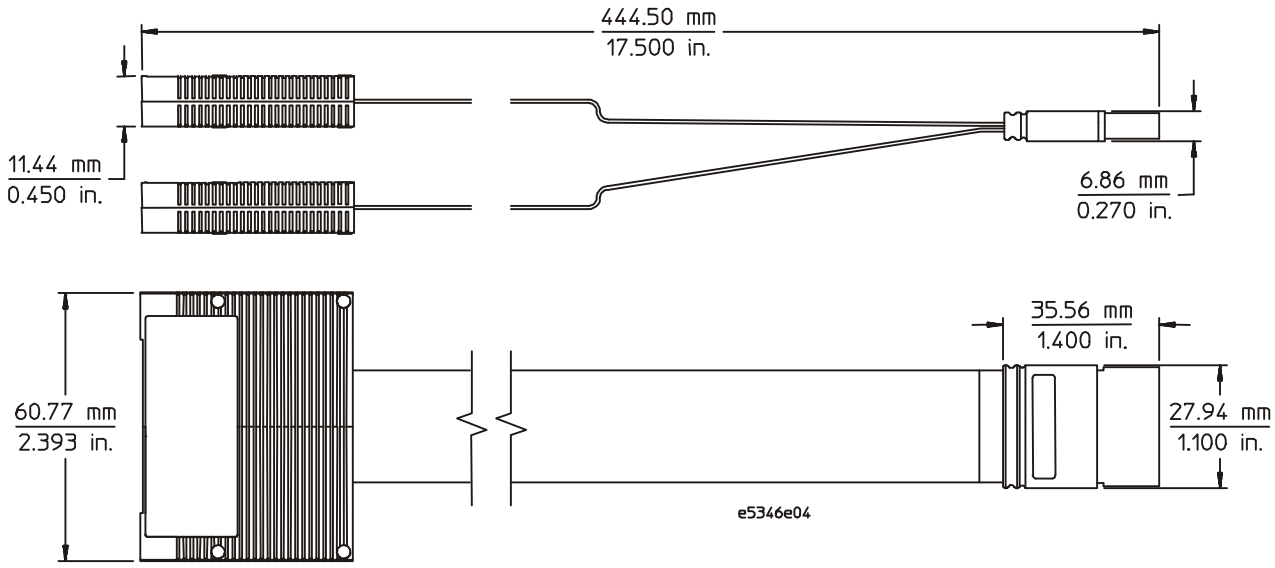
Mictor-38 #3 Pin Number EVEN POD	Logic Analyzer channel number	PCI Signal name
5	CLK/16	unused*
7	15	AD63
9	14	AD62
11	13	AD61
13	12	AD60
15	11	AD59
17	10	AD58
19	9	AD57
21	8	AD56
23	7	AD55
25	6	AD54
27	5	AD53
29	4	AD52
31	3	AD51
33	2	AD50
35	1	AD49
37	0	AD48

***This pin is unused and can be connected to any signal and assigned by the user in the Format menu.**

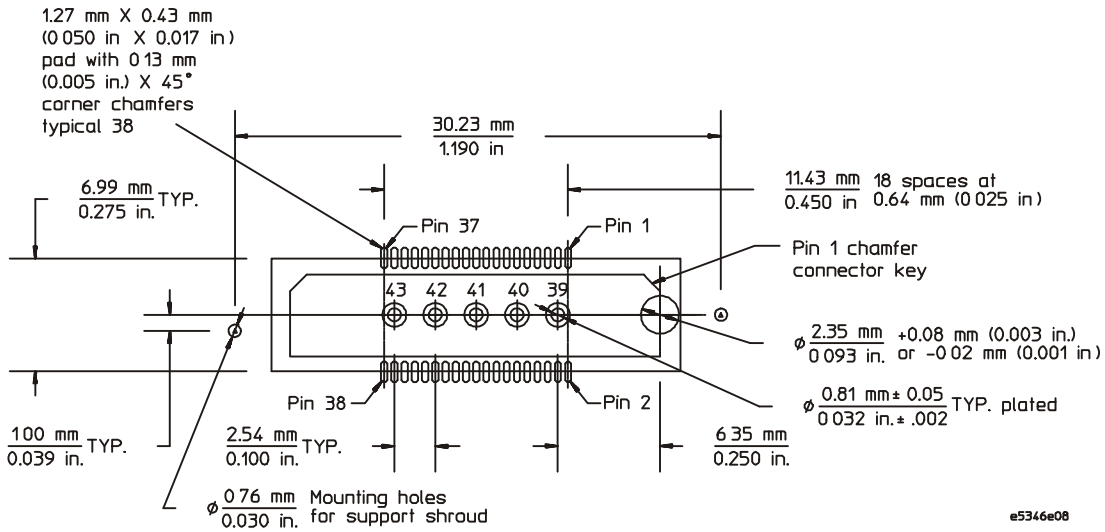
E5346A

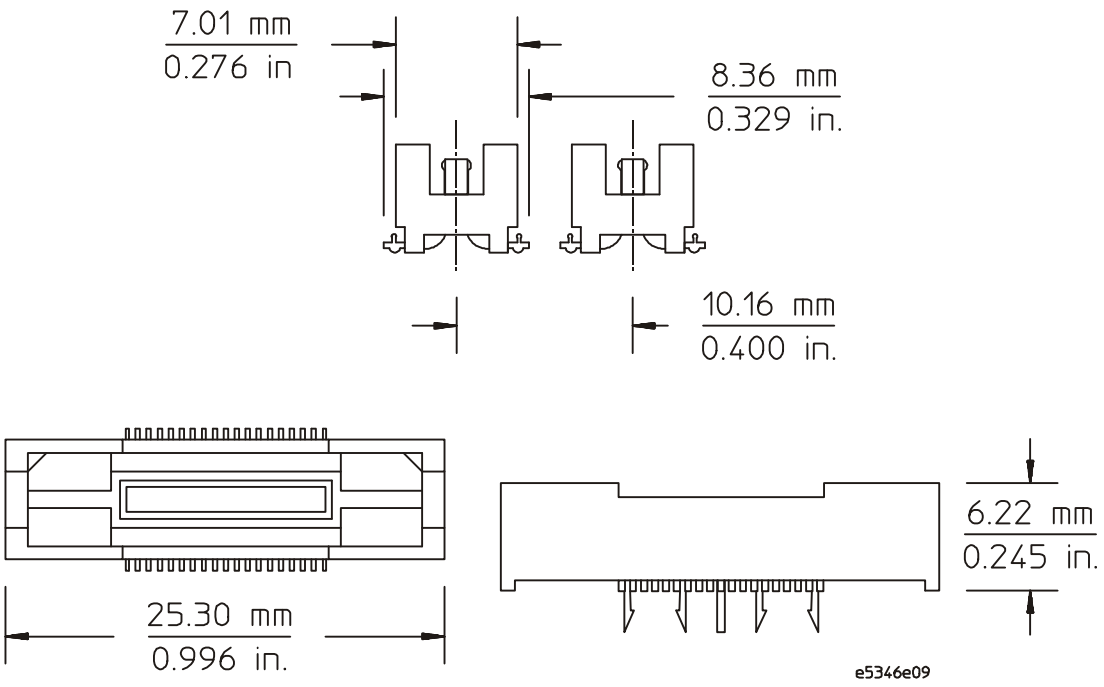

Probe cables
from logic analyzer
Odd # Probes
High density
adapter cables
Even # Probes
Internal
termination
networks
Top view surface mount connector
AMP "Mictor 38" pin assignment
+5VDC 1
GND DC 3
CLK 5
D15 7
D14 9
D13 11
D12 13
D11 15
D10 17
D9 19
D8 21
D7 23
D6 25
D5 27
D4 29
D3 31
D2 33
D1 35
D0 37
GND
2 SCL
4 SDA
6 CLK
8 D15
10 D14
12 D13
14 D12
16 D11
18 D10
20 D9
22 D8
24 D7
26 D6
28 D5
30 D4
32 D3
34 D2
36 D1
38 D0
Optional
shroud
Pin 1
bevel
Mictor

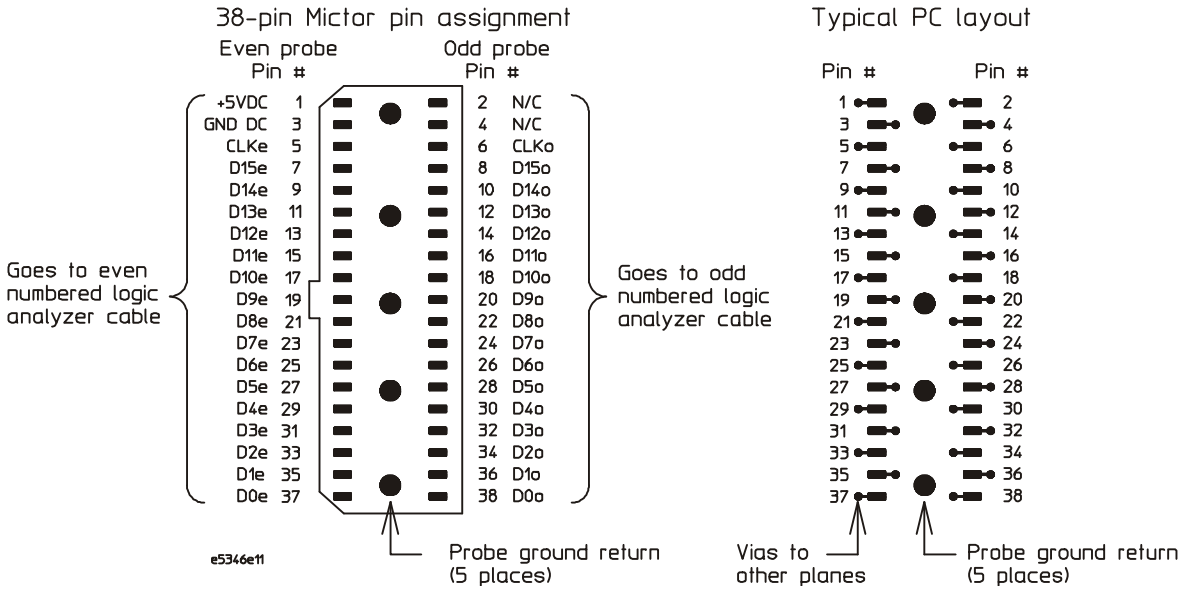
E5346A/E5351A Mechanical Dimensions



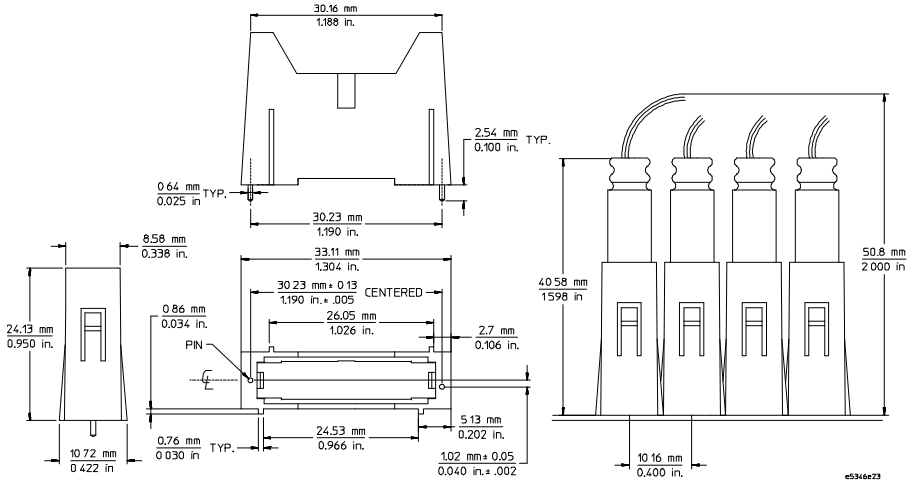
AMP Mictor-38 Connector




7.01 mm
0.276 in
8.36 mm
0.329 in.
10.16 mm
0.400 in.
25.30 mm
0.996 in.
6.22 mm
0.245 in.
e5346e09


38-pin Mictor pin assignment
Even probe
Pin #
Odd probe
Pin #
+5VDC 1
GND DC 3
CLKe 5
D15e 7
D14e 9
D13e 11
D12e 13
D11e 15
D10e 17
D9e 19
D8e 21
D7e 23
D6e 25
D5e 27
D4e 29
D3e 31
D2e 33
D1e 35
D0e 37
2 N/C
4 N/C
6 CLKo
8 D15o
10 D14o
12 D13o
14 D12o
16 D11o
18 D10o
20 D9o
22 D8o
24 D7o
26 D6o
28 D5o
30 D4o
32 D3o
34 D2o
36 D1o
38 D0o
Goes to even numbered logic analyzer cable
Goes to odd numbered logic analyzer cable
Probe ground return (5 places)
e5346e11
Typical PC layout
Pin #
Pin #
1 2
3 4
5 6
7 8
9 10
11 12
13 14
15 16
17 18
19 20
21 22
23 24
25 26
27 28
29 30
31 32
33 34
35 36
37 38
Vias to other planes
Probe ground return (5 places)

Shroud Mechanical Information



Technical Support

For technical support please call 603-471-2734 or e-mail us at tech_sup@futureplus.com